# A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

## BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor integrated circuit device and a manufacturing method thereof, particularly to a technique effective when applied to a semiconductor integrated circuit device using a so-called strained substrate, which is a substrate to which a stress has been applied at a surface portion thereof, and a manufacturing method of the device.

Characteristics of a semiconductor element, such as MISFET (Metal Insulator Semiconductor Field Effect Transistor), formed over the main surface of a semiconductor substrate are determined by various factors. When a tensile stress is applied to the surface layer of the substrate, mobility of electrons in a channel region increases, which improves the current driving capacity of MISFET.

Such a substrate is called "strained substrate". A description of MOSFET using such a substrate can be found, for example, in *Strained Si MOSFETs for High Performance CMOS Technology* (2001 Symposium on VLSI Technoplogy Digest, pp59 to 60).

## SUMMARY OF THE INVENTION

The present inventors are engaged in research and development of a semiconductor integrated circuit device and, in particular, have carried out various investigations on the employment of a strained substrate with a view to improving the characteristics of MISFET.

This strained substrate can be obtained by forming an SiGe film over an Si substrate by epitaxial growth and then forming an Si film over this SiGe film by epitaxial growth. As described later, a tensile stress is applied to the uppermost Si film, influenced by an Si-Ge lattice spacing.

Over the substrate, a plurality of elements are to be formed. In order to isolate them each other, an element isolation made of an insulating film is formed. This element isolation is formed, for example, by making a groove in an element isolation region and then embedding an insulating film in the groove.

For example, an insulating film such as silicon oxide film is deposited by CVD (Chemical Vapor Deposition) over the substrate including the inside of the groove, followed by removal of a portion of the insulating film outside the groove by CMP (Chemical Mechanical Polishing), whereby the insulating film is embedded in the groove.

Direct filling of the CVD insulating film in the groove however accelerates the flow of a leakage current along the groove (walls of the element isolation). This

owes to a rise in an interface state density between the CVD insulating film and semiconductor substrate.

A method of making a groove and then, after thermal oxidation of the inside walls thereof, embedding a CVD insulating film in the groove is therefore adopted.

On a strained substrate having an SiGe film, however, the interface state density of an SiGe oxide film formed upon oxidation of the inside wall of the groove is one order of magnitude greater than that of an Si oxide film.

Accordingly, when a strained substrate is employed, a leakage current becomes greater than that when an Si substrate is used, and in addition, a problem such as a deterioration in element isolating properties occurs.

In order to overcome the above-described problem, disclosed, for example, in Japanese Patent Application Laid-Open No. 275526/1993 (USP5266813) is a technique of preventing leakage by forming a single crystal silicon layer 60 as a groove liner.

A semiconductor integrated circuit device is different in constitution, depending on the degree of improvement of their characteristics or miniaturization requested. Under such a state, the above-disclosed technique is not sufficient for preventing a leakage current, which will be described later in detail.

An object of the present invention is to provide a

technique capable of improving the element isolating properties of a strained substrate, particularly, to reduce a leakage current occurring via the wall of an element isolation even in the case where a well has a high concentration or a conductive film is disposed over the element isolation.

Another object of the present invention is to improve the element isolating properties of a strained substrate, thereby improving the characteristics of the resulting semiconductor integrated circuit formed over the main surface of the substrate and improving the yield of the device.

The above-described and the other objects and novel features of the present invention will be apparent from the description herein and accompanying drawings.

Of the inventions disclosed by the present application, summary of the typical ones will next be described briefly.

According to the semiconductor integrated circuit device of the present invention, an element isolation is formed in a semiconductor substrate having an SiGe layer and a first Si layer formed by epitaxial growth thereover. It has a second Si layer between the element isolation having its bottom in the SiGe layer, and the SiGe layer.

A manufacturing method of a semiconductor integrated

circuit device according to the present invention comprises forming, in an element isolation region of a semiconductor substrate having an SiGe layer and a first Si layer formed thereover by epitaxial growth, a groove which runs through the first Si layer and reaches the SiGe layer; forming thereover a second Si layer; heat treating the substrate to convert a portion of the second Si film corresponding to a predetermined thickness from the surface into a first insulating film, forming over the first insulating film a second insulating film to have a thickness enough to fill therewith the groove, and removing a portion of the second insulating film outside the groove to form a shallow groove isolation.

Alternatively, prior to the formation of the second Si layer, the bottom and side walls of the groove are subjected to thermal oxidation to form an SiGe oxide film and an Si oxide film. After removal of only the SiGe oxide film by etching, the second Si layer may be formed only over the exposed SiGe layer.

A manufacturing method of a semiconductor integrated circuit device, comprises:

(a) preparing a semiconductor substrate having an SiGe layer and a first Si layer epitaxially grown thereover;

(b) etching the semiconductor substrate to form, in

element isolation regions of the semiconductor substrate, grooves which run through the first Si layer and reach the SiGe layer,

(c) forming a second Si layer over the surface of the semiconductor substrate including the bottom and side walls of the grooves,

(d) heat treating the second Si layer to convert a portion of the Si film corresponding to a predetermined thickness from the surface of the layer into a first insulating film,

(e) forming, over the first insulating film, a second insulating film having a thickness enough to embed therewith the grooves and removing a portion of the second insulating film outside the grooves to form element isolations formed in the element isolation regions and element formation regions partitioned by the element isolations, and

(f) forming a semiconductor element in the element formation regions.

A manufacturing method of a semiconductor integrated circuit device as described above, wherein the second Si layer is a single crystal Si film and the above-described step (c) is a step of forming the single crystal Si film by epitaxial growth.

A manufacturing method of a semiconductor integrated

circuit device as described above, wherein the second Si film is a polycrystalline Si film and the above-described step (c) is a step of depositing the polycrystalline Si film over the surface of the semiconductor substrate including the bottom and side walls of each of the grooves.

A manufacturing method of a semiconductor integrated circuit device as described above, further comprises, between the steps (d) and (e):

(g) forming a nitride film over the first insulating film.

A manufacturing method of a semiconductor integrated circuit device as described above, further comprises, between the step (d) and (e):

(g) forming a nitride film over the first insulating film and then, anisotropically etching the nitride film to leave a portion of the nitride film over the side walls of each of the grooves.

A manufacturing method of a semiconductor integrated circuit device as described above, wherein the second insulating film of the step (e) is a silicon oxide film and the silicon oxide film is formed by CVD using ozone and tetraethoxysilane as raw materials.

A manufacturing method of a semiconductor integrated circuit device as described above, wherein the second insulating film of the step (e) is a silicon oxide film and

the silicon oxide film is formed by thermal treatment of a film which has been deposited by CVD using ozone and tetraethoxysilane as raw materials.

A manufacturing method of a semiconductor integrated circuit device as described above, wherein the step (f) is a step of forming an MISFET and the step (f) comprises forming, in the element isolation region, a conductive film of the same layer with a gate electrode constituting the MISFET.

A manufacturing method of a semiconductor integrated circuit device as described above, wherein upon completion of the semiconductor integrated circuit device, the second Si layer remains.

A manufacturing method of a semiconductor integrated circuit device, comprises:

(a) preparing a semiconductor substrate having an SiGe layer and a first Si layer epitaxially grown thereover;

(b) etching the semiconductor substrate to form, in element isolation regions of the semiconductor substrate, grooves which run through the first Si layer and reach the SiGe layer,

(c) subjecting the surface of the semiconductor substrate including the bottom and side walls of each of the grooves to thermal oxidation to form an SiGe oxide film

over the surface of the SiGe layer exposed from the bottom and side walls of each of the grooves and forming an Si oxide film over the surface of the Si layer exposed from the side walls of each of the grooves,

(d) etching the SiGe oxide film at a higher selectivity relative to that of the Si oxide film to expose the SiGe layer from the bottom and side walls of each of the grooves,

(e) forming by epitaxial growth a second single crystal Si layer over the surface of the SiGe layer exposed by the step (d),

(f) heat treating the second Si layer to convert a portion of the Si film corresponding to a predetermined thickness from the surface of the layer into a first insulating film,

(g) forming over the first insulating film a second insulating film to have an enough thickness to embed therewith the grooves and removing a portion of the second insulating film outside the grooves to form element isolations formed in the element isolation regions and element formation regions partitioned by the element isolations, and

(h) forming a semiconductor device in the element formation regions.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a fragmentary cross-sectional view of a substrate illustrating a manufacturing method of a semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 2 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 3 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 4 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 5 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 6 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 7 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 8 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 9 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 10 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 11 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 12 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 13 is a fragmentary cross-sectional view of a

substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 14 is a fragmentary plan view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 1 of the present invention;

FIG. 15 is a fragmentary cross-sectional view of a substrate of the semiconductor integrated circuit device for explaining an advantage of Embodiment 1 of the present invention;

FIG. 16 is a fragmentary cross-sectional view of a substrate of the semiconductor integrated circuit device for explaining another advantage of Embodiment 1 of the present invention;

FIG. 17 is a fragmentary cross-sectional view of a substrate of the semiconductor integrated circuit device for explaining a further advantage of Embodiment 1 of the present invention;

FIG. 18 is a fragmentary plan view of a substrate of the semiconductor integrated circuit device for explaining the further advantage of Embodiment 1 of the present invention;

FIG. 19 is a fragmentary cross-sectional view of a substrate of the semiconductor integrated circuit device

for explaining the further advantage of Embodiment 1 of the present invention;

FIG. 20 is a fragmentary cross-sectional view of a substrate illustrating a manufacturing method of a semiconductor integrated circuit device according to Embodiment 2 of the present invention;

FIG. 21 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 2 of the present invention;

FIG. 22 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 2 of the present invention;

FIG. 23 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 2 of the present invention;

FIG. 24 is a fragmentary cross-sectional view of a substrate illustrating s manufacturing method of a semiconductor integrated circuit device according to Embodiment 3 of the present invention;

FIG. 25 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to

Embodiment 3 of the present invention;

FIG. 26 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 3 of the present invention;

FIG. 27 is a fragmentary cross-sectional view of a substrate illustrating another manufacturing method of the semiconductor integrated circuit device according to Embodiment 3 of the present invention;

FIG. 28 is a fragmentary cross-sectional view of a substrate illustrating the another manufacturing method of the semiconductor integrated circuit device according to Embodiment 3 of the present invention;

FIG. 29 is a fragmentary cross-sectional view of a substrate illustrating a manufacturing method of a semiconductor integrated circuit device according to Embodiment 4 of the present invention;

FIG. 30 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 4 of the present invention;

FIG. 31 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 4 of the present invention;

FIG. 32 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 4 of the present invention; and

FIG. 33 is a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated circuit device according to Embodiment 4 of the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will hereinafter be described specifically based on accompanying drawings. In all the drawings for describing the below-described embodiments, elements having like function will be identified by like reference numerals and overlapping descriptions will be omitted.

(Embodiment 1)

A semiconductor integrated circuit device according to this Embodiment will next be described in line with its manufacturing steps.

FIGS. 1 to 13 are each a fragmentary cross-sectional view of a substrate illustrating a manufacturing method of a semiconductor integrated circuit device according to this Embodiment. FIG. 14 is a fragmentary plan view of the substrate and each cross-sectional view is a view taken

along a line A-A of the plan view. The nMIS-A is the formation region of an n-channel type MISFET, while the pMIS-A is the formation region of a p-channel type MISFET.

Prepared first is a semiconductor substrate (which will hereinafter be called "substrate", simply) having, as illustrated in FIG. 1, a single crystal silicon (Si) layer 1a, an SiGe (silicon germanium) layer 1b, and a single crystal Si layer 1c epitaxially grown thereover.

This substrate 1 is formed as follows. First, the SiGe layer 1b of about 5 μm thick is formed over the surface of the single crystal Si substrate 1a by epitaxial growth while using Si and Ge at a composition ratio (Si:Ge) of, for example, 0.8:0.2. Then, the Si layer 1c of about 0.02 μm is formed over the SiGe layer 1b by epitaxial growth.

A tensile stress is applied to the Si layer 1c of such a substrate 1. The lattice spacing of the SiGe layer 1b is wider than that of the single crystal Si so that the Si layer grown over the SiGe layer 1b has a widened lattice spacing, influenced by that of the SiGe layer. Although this widening of the lattice spacing is relaxed as the growth of the film proceeds, a tensile stress is applied to the Si layer 1c and mobility of carriers increases when the lattice spacing of the Si layer is wider than that of the general Si crystal over the surface of the substrate. It

is only necessary that a layer underlying the Si layer 1c has crystals wider in lattice spacing than Si and permits epitaxial growth of Si from the surface of the layer. This substrate 1 is called "strained substrate", while the Si layer 1c is called "strained layer".

A shallow groove isolation SGI as an element isolation is then formed in the substrate 1. This shallow groove isolation SGI is formed, as illustrated in FIG. 2, by forming a silicon oxide film 21 of about 10 nm thick over the surface of the substrate 1 and then, depositing a silicon nitride film 22 of about 150 nm over the silicon oxide film.

With an unillustrated photoresist film (which will hereinafter be called "resist film", simply) as a mask, the silicon nitride film 22 and silicon oxide film 21 are removed from the element isolation regions (ISOp-p, ISOp-n) of the substrate 1.

After removal of the resist film, the substrate 1 is etched with the silicon nitride film 22 as a mask to form a groove 2. The groove 2 must have a depth of about 300 nm in this case in order to maintain element isolating properties. This groove 2 rungs through the Si layer 1c and reaches the SiGe layer 1b. The bottom of the groove 2 exists in the SiGe layer 1b.

Accordingly, the Si layer 1c and SiGe layer 1b are

exposed from the side walls of the groove 2, while the SiGe layer 1b is exposed from the bottom of the groove 2.

Reduction, for example, heat treatment in a hydrogen atmosphere is then conducted to remove a natural oxide film from the surface of the groove 2. As illustrated in FIG. 3, single crystal Si is epitaxially grown over the Si layer 1c and SiGe layer 1b of the side walls of the groove and over the SiGe layer 1b of the bottom of the groove 2, whereby a single crystal Si film 3 of about 20 nm thick is formed. At the upper portion of the side walls of the groove 2, single crystal Si grows not only horizontally but also vertically, relative to the surface of the substrate, which means growth of single crystal Si to form a protrusion, at the upper portion of the side walls of the groove, from the surface of the substrate 1.

Then, an Si oxide film (thermal oxide film) 6 is to be formed by oxidizing the surface of the Si film 3 on the inside wall of the groove 2. Prior thereto, the silicon oxide film 21 is selectively etched to retreat it from the side walls of the groove as illustrated in FIG. 4.

As illustrated in FIG. 5, the surface of the Si film 3 on the inside wall of the groove 2 is oxidized to form an Si oxide film (thermal oxide film) 6. This Si oxide film 6 is formed for the purpose of (1) suppressing generation of crystal defects which will otherwise occur owing to stress

concentration to a corner portion (a1) on the bottom of the groove by rounding the Si oxide film 6 on the corner portion; and (2) suppressing fluctuations in the characteristics of a semiconductor element which will otherwise occur owing to electric field concentration to a corner portion (a2) at the upper portion of the side walls of the groove by rounding the Si oxide film 6 on the corner portion. When a CVD insulating film to be embedded inside of the groove is brought into direct contact with the Si layer (1a), an interface state density increases. The Si oxide film (thermal oxide film) 6 capable of suppressing an interface state density even if they are brought into contact is interposed (3) for the purpose of keeping an increase in interface state density small.

According to this Embodiment, oxidation is conducted after the silicon oxide film 2 is retreated from the side wall portions of the groove 2 (FIG. 4). This enables to enlarge the bird's beak and ease the angle of the corner, whereby electric field concentration can be relaxed further.

Upon this oxidation, a portion of the Si film 3 corresponding to a predetermined thickness from its surface is oxidized so that the Si film 3 partly remains even after oxidation. For example, since oxidation of Si forms an Si oxide film twice as much volume as that of Si, oxidation of 10 nm of the Si film 3 having a thickness of 20 nm forms

the Si oxide film 6 of about 20 nm thickness and leaves the Si film 3 of about 10 nm thick.

As illustrated in FIG. 6, a silicon oxide film 7 is deposited as an insulating film by CVD (Chemical Vapor Deposition) over the substrate 1 including the inside (over the Si oxide film 6) of the groove 2. This silicon oxide film can be formed, for example, by CVD using tetraethoxysilane ($Si(OC_2H_5)_4$) and ozone ($O_3$) as raw materials. Such a film is called "ozone TEOS ($O_3$-TEOS) film". The $O_3$-TEOS film is then heat treated (densified) to remove impurities therefrom to obtain a dense film. The formation method of the silicon oxide film 7 is not limited to the above-described one, but HDP (High Density Plasma) CVD can be employed instead. This method does not need densification.

As illustrated in FIG. 7, the silicon oxide film 7 is polished, for example, by CMP (Chemical Mechanical Polishing) until the silicon nitride film 22 is exposed therefrom, whereby the surface of the silicon oxide film is planarized.

As illustrated in FIG. 8, the silicon nitride film 22 is removed. As a result, the Si film 3 on the inside wall of the groove 2 and a shallow groove isolation SGI made of the Si oxide film 6 and silicon oxide film 7 are completed. A region surrounded by this shallow groove isolation SGI

becomes an element formation region (refer to FIG. 14). After the removal of the silicon nitride film 22, the silicon oxide film 7 on the surface of the shallow groove isolation SGI protrudes from the surface of the substrate 1, but this protrusion of the shallow groove isolation SGI disappears gradually by the subsequent steps such as cleaning of the substrate and removal of the thermal oxide film.

With regards to the shallow groove isolation SGI, the width H2 of the shallow groove isolation on the boundary between an n channel type MISFET formation region (nMIS-A) and a p channel type MISFET formation region (pMIS-A) is greater than the width H1 of the shallow groove isolation in the n-channel MISFET formation region (nMIS-A). The shallow groove isolation having the width H1 will be an isolation in a p type well 4p which will be described later so that it is called "intra-well isolation (ISOp-p)", while that having the width H2 will be an isolation between the p type well 4p and an n type well 4n so that it is called "well-well isolation (ISOn-p)". The width H1 of the intra-well isolation is about 0.2 μm, while the width H2 of the well-well isolation is about 0.4 μm.

As illustrated in FIG. 9, for example, boron is ion-implanted as a p type impurity at a dose of about $2 \times 10^{13}$ $cm^{-2}$ in the n channel MISFET formation region (nMIS-A) of

the substrate 1. In the p channel MISFET formation region (pMIS-A) of the substrate 1, on the other hand, phosphorus is ion-implanted as an n type impurity at a dose of about 2 $\times 10^{13}$ $cm^{-2}$. Heat treatment is then conducted to diffuse these impurities, whereby n type well 4n and p type well 4p are formed. These n type well 4n and p type well 4p each has a depth of about 450 nm and the n type well 4n and p type well 4p each has a bottom in the SiGe layer 1b. The bottom of these n type well 4n and p type well 4p exist at a position deeper than the bottom of the shallow groove isolation SGI. In this case, the well has a maximum concentration of about 2 $\times 10^{18}$ $cm^{-3}$.

After wet cleaning of the surface of the substrate 1 (p type well 4p and n type well 4n) with, for example, a hydrofluoric acid detergent, a gate oxide film (gate insulating film) 8 of about 2 nm thick is formed on the surface of each of the p type well 4p and n type well 4n by thermal oxidation.

Over the gate oxide film 8, a low resistance polycrystalline silicon film 9 of about 150 nm thick is formed as a conductive film by CVD. Then, with an unillustrated film as a mask, the polycrystalline silicon film 9 is etched to form a gate electrode G.

A gate electrode G is also formed over the shallow groove isolations SGI (ISOp-p, ISOp-n). A gate electrode

over another un-illustrated element formation region may extend even over the shallow groove isolation SGI. The polycrystalline silicon film (9), which is the same layer with the gate electrode G, may be formed over the shallow groove isolation as an interconnect or resistor.

As illustrated in FIG. 10, for example, arsenic (As) is implanted as an n type impurity to both sides of the gate electrode G of the p type well 4p, whereby $n^-$ type semiconductor regions 11 are formed. In a similar manner, a p type impurity is implanted to both sides of the gate electrode G of the n type well 4n, whereby $p^-$ type semiconductor regions 12 are formed.

As illustrated in FIG. 11, a silicon nitride film of about 70 nm thick is deposited over the substrate 1 by CVD, followed by anisotropic etching to form side wall spacers 13 of about 50 nm thick over the side walls of the gate electrode G.

Then, for example, arsenic is implanted as an n type impurity to both sides of the gate electrode G over the p type well 4p, and for example, boron fluoride is implanted as a p type impurity to both sides of the gate electrode G over the n type well 4n, followed by heat treatment at 1000 °C for 1 second to activate these impurities, whereby $n^+$ type semiconductor regions 14 and $p^+$ type semiconductor regions 15 (source, drain) are formed.

These $n^+$ type semiconductor regions 14 and $p^+$ type semiconductor regions 15 (source, drain) extend even to the SiGe layer 1b. These regions may have a bottom in the Si layer 1c by reducing their depth. To enlarge the tensile stress of the Si layer 1c, however, a decrease in the thickness of the Si layer 1c as much as possible is desired. In such a case, the $n^+$ type semiconductor regions 14 and $p^+$ type semiconductor regions 15 (source and drain) will extend to the SiGe layer 1b.

By the steps so far described, an N channel type MISFETQn and a p channel type MISFETQp having an LDD (Lightly Doped Drain) structure and equipped with sources and drains ($n^-$ type semiconductor regions, $n^+$ type semiconductor regions, $p^-$ type semiconductor regions, and $p^+$ type semiconductor regions) are formed. FIG. 14 is a fragmentary cross-sectional view of a substrate of the semiconductor integrated circuit device according to this Embodiment.

In this Embodiment, the MISFET is formed over the strained substrate 1 so that a mobility of electrons in a channel region can be improved, which results in an improvement in the current driving capacity of the MISFET, particularly, the current driving capacity of the n channel type MISFET.

In this Embodiment, the Si film 3 is formed between

the shallow groove isolation SGI and the SiGe layer 1b so that an interface state density on the interface between the shallow groove isolation SGI and Si film 3 can be reduced, leading to a reduction in the leakage current flowing via the interface.

As illustrated in FIG. 15, it is possible to form an Si oxide film 6a and an SiGe oxide film 6b by directly oxidizing the side walls and bottom of the groove 2. Considering that the SiGe oxide film 6b has an interface state density of about one order of magnitude greater than that of the Si oxide film, direct oxidization of the inside wall of the groove 2 is insufficient as a countermeasure against leakage current. In other words, as illustrated in FIG. 15, electrons become apt to be trapped around the shallow groove isolation (SiGe oxide film 6b), which causes a leakage current to flow along the wall of the shallow groove isolation.

According to this Embodiment, on the other hand, no SiGe oxide film 6b exists on the interface between the shallow groove isolation SGI and the SiGe layer 1b so that a leakage current can be reduced. In addition, contact between the CVD insulating film (7) and the substrate can be avoided by the Si oxide film 6 formed by oxidizing the Si film 3, which has been formed over the inside wall of the groove 2, whereby an interface state density between

them can be reduced.

Since the Si film 3 is left on the inside wall of the groove 2 even after the formation of the Si oxide film 6, a contact does not occur between the Si oxide film 6 and the SIGe layer 1b, whereby an interface state density therebetween can be reduced.

Even if the Si oxide film 6 is oxidized further by the heat treatment after formation of the Si oxide film 6, for example, densification of the $O_3$-TEOS film (7) or activation of impurities constituting the source and drain (14 and 15), the remaining Si film 3 is oxidized as needed, whereby the oxidation of the SiGe layer 1b can be prevented. This leads to suppression of a rise in the interface state density which will otherwise occur by the existence of the SiGe oxide film.

As in this Embodiment, when the well has a relatively high concentration (for example, $1 \times 10^{18}$ $cm^{-3}$ or greater) or a conductive film (gate electrode) is formed over the shallow groove isolation, electrons become apt to be trapped at the periphery of the shallow groove isolation SGI as illustrated in FIG. 16.

Over the shallow groove isolation, a parasitic MOS transistor is formed by the conductive film (gate electrode) and shallow groove isolation SGI. When a potential is applied to the conductive film, electrons are

accumulated on the outside wall of the shallow groove isolation and, application of a potential exceeding a threshold potential (Vt) of the parasitic MOS to the conductive film turns the parasitic MOS transistor on. It is generally known that the higher the well concentration, the higher the interface state density of a thermal oxide film formed thereover.

This Embodiment is therefore more effective when used in such a case (where the well has a relatively high concentration, or the gate electrode is formed over the shallow groove isolation).

As illustrated in FIG. 17, even if the shallow groove isolations SGI (6 and 7) are surrounded, at the periphery thereof, with the Si film 3, a channel for leakage current is limited when the shallow groove isolation SGI has a bottom at a position deeper than the SiGe layer 1b.

Electrons trapped on the interface between the shallow groove isolation SGI and the SiGe layer 1b flow via a hatched portion of FIG. 18. FIG. 18 is a fragmentary plan view of the substrate of the semiconductor integrated circuit device illustrated in FIG. 17 and FIG. 17 corresponds to a cross-section taken along a line A-A of FIG. 18.

When the bottom of the shallow groove isolation SGI exists in the SiGe layer 1b as in this Embodiment (refer to

FIG. 1), a leakage current happens to occur via the bottom of the shallow groove isolation SGI as shown by the hatched portion of FIG. 19 so that a countermeasure against the leak current becomes important.

The shallow groove isolation SGI tends to be shallow, reflecting the miniaturization of the element. This is partly because when a pattern area becomes small, an aspect ratio (depth of a groove/pattern width) increases, resulting in a deterioration in the embedding property of an insulating film.

When the bottom of the shallow groove isolation SGI exists in the SiGe layer 1b, this Embodiment can be used suitably.

As illustrated in FIG. 12, a metal film such as a Co (cobalt) film is deposited over the substrate 1, followed by heat treatment to cause a silicidation reaction at the contact portion of the metal film with each of the gate electrode G and substrate 1, whereby $CoSi_2$ (cobalt silicide film) 17 is formed in self alignment. Then, an unreacted portion of the Co film is removed, followed by heat treatment.

As illustrated in FIG. 13, a silicon oxide film 19 is then deposited by CVD over the substrate 1 as an interlayer insulating film and is planarized at the surface thereof as needed. The silicon oxide film 19 over the source and

drain (15 and 14) and gate electrode of the MISFETS (Qn and Qp) are etched to form contact holes C1. The contact hole over the gate electrode is not illustrated.

Over the silicon oxide film 19 including the inside of the contact hole C1, W (tungsten film) is deposited, for example, as a conductive film. The W film outside the contact hole C1 is polished and removed by CMP, whereby a plug P1 is formed.

Over the silicon oxide film 19 including the plug P1, a W film, for example, as a conductive film is deposited, followed by patterning into a desired shape to form a first-level interconnect M1 is formed.

By repeating these steps for the formation of the interlayer insulating film, plug and interconnect, a multilevel interconnect can be formed, but illustration and detailed formation steps thereof are omitted.

Then, a protective film having an opening at the pad portion is formed over the uppermost-level interconnect and the substrate 1 in the form of a wafer is diced into a plurality of chips.

The pad portion and external lead are connected by a bump electrode or wire and if necessary, the chip is sealed, at the periphery thereof, with a resin, whereby a semiconductor integrated circuit device is completed.

Even after completion of the semiconductor integrated

circuit device, it is preferred that the Si film 3 remains.

(Embodiment 2)

In Embodiment 1, a single crystal Si film formed by epitaxial growth is used as the Si film 3. Alternatively, a polycrystalline silicon film is usable.

The semiconductor integrated circuit device of this Embodiment will next be described in line with its manufacturing steps.

FIGS. 20 to 23 are fragmentary cross-sectional views of a substrate each illustrating the manufacturing method of the semiconductor integrated circuit device according to this Embodiment. Steps until the formation of the groove 2 are similar to those described in Embodiment 1 based on FIGS. 1 and 2, so that a description on it is omitted.

As illustrated in FIG. 20, a polycrystalline silicon film 203 of about 20 nm thick is deposited by CVD over the strained substrate 1 having the groove 2 formed therein. Indicated at numeral 21 is a silicon nitride film, while 22 a silicon nitride film.

As illustrated in FIG. 21, the surface of the polycrystalline silicon film 203 is oxidized to form an Si oxide film (thermal oxide film) 206. Upon this oxidation, a portion of the Si film 203 corresponding to a predetermined thickness from the surface thereof is oxidized. So, even after this oxidation, an unoxidized

portion of the Si film 203 remains. For example, of the Si film 203 having a thickness of 20 nm, the upper 10 nm portion is oxidized to form an Si oxide film 206 of about 20 nm thick and the lower 10 nm portion of the Si film 203 is left unoxidized. This oxidation rounds the Si oxide film 206 existing at a corner portion (a1) on the bottom of the groove. As a result, generation of crystal defects owing to stress concentration to the corner portion can be suppressed.

As illustrated in FIG. 22, a silicon oxide film 7 is deposited as an insulating film by CVD over the substrate 1 (over the Si oxide film 206) including the inside of the groove 2. This silicon oxide film is, for example, an $O_3$-TEOS film as described in Embodiment 1. The $O_3$-TEOS film is then heat treated in an oxygen atmosphere in order to remove impurities in the film and densify the film.

As illustrated in FIG. 23, the silicon oxide film 7 is polished, for example, by CMP until the silicon nitride film 22 appears, whereby the surface of the silicon oxide film is planarized. Then, the silicon nitride film is removed.

As a result, the Si film 203 inside of the groove 2a and a shallow groove isolation SGI made of the Si oxide film 206 and the silicon oxide film 7 are completed. A region surrounded by this shallow groove isolation SGI will

serve as an element formation region (refer to FIG. 14). The surface of the shallow groove isolation SIG will retreat gradually. The intra-well isolation (ISOp-p) has a width H1 of, for example, about 0.2 μm. The width H2 of the well-well isolation (ISOn-p) is greater than the width H1 and is, for example, about 0.4 μm.

In the element formation region, MISFETs (Qn and Qp) are then formed. Subsequent formation steps are similar to those as described in Embodiment 1 based on FIGS. 9 to 14, so detailed explanation is omitted.

This Embodiment also brings about similar effects to those of Embodiment 1. An interface state density between the shallow groove isolation SGI and substrate 1 is considered to be smaller via the single crystal Si film of Embodiment 1 than via the polycrystalline silicon film. (Embodiment 3)

In Embodiments 1 and 2, the CVD insulating film (7) was deposited directly over the Si oxide film (6 or 206), but it is possible to dispose therebetween a silicon nitride film.

The semiconductor integrated circuit device of this Embodiment will next be described in line with its manufacturing steps. FIGS. 24 to 28 are each a fragmentary cross-sectional view of a substrate illustrating the manufacturing method of the semiconductor integrated

circuit device of this Embodiment. Steps until the formation of the Si oxide film 6 are similar to those of Embodiment 1 as described based on FIGS. 1 to 5 so that an explanation on them will be omitted. As described in detail in Embodiment 1 (FIG. 5), the Si oxide film 6 existing at the corner portion (a1) on the bottom of the groove or that existing at the corner portion (a2) at the upper portion of the side walls of he groove are rounded, which are however illustrated in FIG. 24 only simply.

(1) Over the strained substrate 1 having the Si oxide film 6 formed thereover, a silicon nitride film 306 of about 10 nm thick is deposited using CVD as illustrated in FIG. 24. Indicated at numeral 21 is a silicon oxide film and 22 a silicon nitride film.

As illustrated in FIG. 25, over the substrate 1 (over the silicon nitride film 306) including the inside of the groove 2, a silicon oxide film 7 is deposited as an insulating film by CVD. This silicon oxide film is, for example, an $O_3$-TEOS film as explained in Embodiment 1. Then, the $O_3$-TEOS film is heat treated in an oxygen atmosphere to remove impurities therefrom and to densify the film.

As illustrated in FIG. 26, the silicon oxide film 7 is polished, for example, by CMP until the silicon nitride film 22 is exposed and the surface of the silicon oxide

film is planarized. Then, the silicon nitride film 22 is removed.

As a result, the Si film 3 inside wall of the groove 2, and a shallow groove isolation SGI made of the Si oxide film 6, silicon nitride film 306 and silicon oxide film 7 are completed. A region surrounded by this shallow groove isolation SGI is to be an element formation region (refer to FIG. 14). The surface of the shallow groove isolation SIG will retreat gradually. The intra-well isolation (ISOp-p) has a width H1 of, for example, about 0.2 μm. The width H2 of the well-well isolation (ISOn-p) is greater than the width H1 and is, for example, about 0.4 μm.

In the element formation region, MISFETs (Qn, Qp) are then formed. Subsequent formation steps are similar to those as described in Embodiment 1 based on FIGS. 9 to 14, so a detailed explanation is omitted.

This embodiment brings about similar effects to those of Embodiment 1. In addition, since the silicon nitride film 306 is formed over the Si oxide film 6, progress of oxidation of the Si oxide film 6 which will otherwise occur owing to heat treatment after the formation of the Si oxide film 6, for example, densification of the $O_3$-TEOS film (7) as explained in detail in Embodiment 1 or activation of impurities constituting the source and drain (14 and 15) can be suppressed. This makes it possible to suppress

oxidation of the Si film 3, thereby leaving the Si film 3 without failure. When the oxidation of the Si oxide film 6 proceeds, volumetric expansion occurs, whereby a stress is applied to the shallow groove isolation and crystal defects tend to occur. Formation of the silicon nitride film 306 reduces the influence of the stress, thereby preventing the generation of crystal defects.

(2) After deposition of the silicon nitride film 306 of about 10 nm thick by CVD over the strained substrate 1 having the Si oxide film 6 formed thereon, the silicon nitride film may be anisotropically etched as illustrated in FIG. 27 to leave the silicon nitride film 306a only on the side wall portions of the groove 2. The Si oxide film 6 existing at the corner portions (a1 and a2) of the groove is rounded, but such portions are illustrated only simply in FIG. 27.

Then, as in the case (1), after deposition of a silicon oxide film 7 by CVD as an insulating film over the substrate 1 including the inside of the groove 2, the silicon oxide film 7 is polished until the silicon nitride film 22 is exposed, whereby the surface of the silicon oxide film is planarized (FIG. 28). Then, the silicon nitride film 22 is removed.

Even by leaving the silicon nitride film 306a only on the side wall portions of the groove, progress of the

oxidation of the Si oxide film 6 can be suppressed. In other words, since the bottom of the groove is covered by the thick silicon oxide film 7, the progress of the oxidation of the Si oxide film 6 is considered to be slow. Accordingly, by leaving the silicon nitride film 306a only on the side wall portions of the groove which are easily influenced by oxidation, the oxidation of the Si film 3 can be suppressed. In addition, crystal defects can be reduced.

In this Embodiment, formation of the nitride film over the Si oxide film 6 was described in reference to Embodiment 1, but the nitride film can be formed over the Si oxide film 206 of Embodiment 2 in similar steps.

(Embodiment 4)

A semiconductor integrated circuit device of this Embodiment will be described in line with its manufacturing steps. FIGS. 29 to 33 are fragmentary cross-sectional views of the substrate illustrating the manufacturing method of the semiconductor integrated circuit device of this Embodiment. Steps until the formation of the groove 2 are similar to those of Embodiment 1 as described based on FIGS. 1 and 2 so that a description on them is omitted.

First, the surface of the strained substrate 1 having the groove 2 formed therein is oxidized to form an Si oxide film 402a and an SiGe oxide film 402b as illustrated in FIG. 29. These oxide films each has a thickness of about 20 nm.

As illustrated in FIG. 30, only the SiGe oxide film 402b is selectively removed using, for example, $H_2O$ (water), while the Si oxide film 402b is left. This means that the SiGe oxide film 402b is etched under the conditions of a high selectivity relative to the Si oxide film. The SiGe oxide film is water soluble so that it can be removed easily.

As a result, with regards to the inside wall of the groove 2, only the SiGe layer 1b is exposed therefrom and the Si layer 1c is covered with the Si oxide film 402a.

A natural oxide film over the surface of the SiGe layer 1b exposed from the groove is then removed by reduction, for example, heat treatment in a hydrogen atmosphere. As illustrated in FIG. 31, single crystal Si is epitaxially grown over the exposed SiGe layer 1b to form an Si film 403 of about 20 nm thick. Growth of Si does not occur over the Si layer 1c on the side walls of the groove, because the Si oxide film 402a remains on the Si layer.

As illustrated in FIG. 32, the surface of the Si film 403 over the inside wall of the groove 2 is oxidized to form an Si oxide film (thermal oxide film) 406.

As illustrated in FIG. 33, a silicon oxide film 7 is deposited by CVD as an insulating film over the substrate 1 including the inside of the groove 2 (over the Si oxide films 402a and 406). This silicon oxide film is, for

example, an $O_3$-TEOS film as described in Embodiment 1. The $O_3$-TEOS film is then heat treated in an oxygen atmosphere in order to remove impurities in the film and densify the film.

The silicon oxide film 7 is then polished, for example, by CMP until the silicon nitride film 22 appears, whereby the surface of the silicon oxide film is planarized. Then, the silicon nitride film 22 is removed.

As a result, the Si film 403 inside of the groove 2, and a shallow groove isolation SGI made of the Si oxide films 402a and 406 and silicon oxide film 7 are completed. A region surrounded by this shallow groove isolation SGI will serve as an element formation region (refer to FIG. 14). The surface of the shallow groove isolation SIG will retreat gradually. The intra-well isolation (ISOp-p) has a width H1 of, for example, about 0.2 μm. The width H2 of the well-well isolation (ISOn-p) is greater than the width H1 and is, for example, about 0.4 μm.

In the element formation region, MISFETs (Qn, Qp) are then formed. Subsequent formation steps are similar to those as described in Embodiment 1 based on FIGS. 9 to 14, so a detailed explanation on them is omitted.

This Embodiment also brings about similar effects to those of Embodiment 1. In addition, in this Embodiment, Si is epitaxially grown only over the SiGe layer 1b inside of

the groove with the Si oxide film 402a as a mask so that in the Si film 403, no boundary exists between a portion grown from the Si layer 1c and a portion grown from the SiGe layer 1b (refer to FIG. 3). This brings about an improvement in the film quality.

If there exists such a boundary in the Si layer, surface discontinuity appears in the crystal lattice, which presumably causes crystal defects.

This Embodiment, however, can avoid formation of surface discontinuity in the Si film 403, thereby reducing the crystal defects of the remaining Si film 403.

Embodiment 3 may be applied to this Embodiment, in other words, a silicon nitride film may be formed over the Si oxide film 406 of this Embodiment.

The invention made by the present inventors was described specifically based on some embodiments. It should however be borne in mind that the present invention is not limited to the above-described embodiments, but can be modified within an extent not departing from the gist of the invention.

In the above embodiments, the invention was applied to the case where MISFET is formed, but it is applicable not only to it, but also to semiconductor integrated circuit devices having the other semiconductor device, for example, bipolar transistor, and a current channel and

element isolation on the surface of the substrate.

Advantages of the typical inventions, of the inventions disclosed by the present application, will next be described briefly.

A shallow groove isolation is made of a groove, which is formed in an isolation region of a strained substrate having an SiGe layer and a first Si layer formed thereover by epitaxial growth, and an insulating film inside of the groove. Since a second Si layer is formed between the shallow groove isolation which penetrates the first Si layer and has its bottom in the SiGe layer and the SiGe layer, element isolating properties of the strained substrate can be improved. In addition, the characteristics of a semiconductor integrated circuit formed over the main surface of the strained substrate can be improved. Moreover, the yield of the device can be improved.

In particular, even in the case when a well has a high concentration or a conductive film is disposed over the shallow groove isolation, a leakage current via the shallow groove isolation can be reduced, leading to an improvement in element isolating properties.